CLAIMS

What is claimed is:

1. A computer aided method of designing a circuit comprising:

selecting a circuit block of the circuit, the circuit block having a plurality of block inputs;

deriving a fan-in cone function for each block input of the plurality, each fan-in cone function comprising a corresponding block input variable expressed as a function of at least one fan-in cone variable;

conjoining the fan-in cone functions for each block input into a circuit block constraint function; and

quantifying the circuit block constraint function to provide at least one circuit block constraint as a function of block input variables.

2. The method of claim 1 wherein the selecting the circuit block comprises one of:

selecting the circuit block by a user; and

selecting the circuit block by a design tool along predefined circuit design partitions.

3. The method of claim 1 wherein the deriving a fan-in cone function for each block input of the plurality comprises:

selecting a block input; and

backtracing each circuit branch from the selected block input to a node of a type corresponding to a cone stop node.

4. The method of claim 3 wherein the cone stop node is at least one of the group consisting of a latch output, a primary circuit input, a memory output, and an intermediate circuit node if such intermediate circuit node is common to a plurality of fan-in cones corresponding to the selected circuit block.

5. The method of claim 1 wherein the deriving a fan-in cone function for each block input of the plurality comprises:

defining each block input variable to be equivalent to a logical function of fan-in cone variables of a fan-in cone corresponding to the block input variable, the logical function depending on circuitry in a backtraced circuit branch.

6. The method of claim 1 wherein the conjoining the fan-in cone functions for each block input into a circuit block constraint function comprises defining the circuit block constraint function to be equal to the fan-in cone functions ANDed together.

7. The method of claim 1 wherein the quantifying the circuit block constraint function comprises:

selecting a fan-in cone variable of the circuit block constraint function;

generating a first instance of the circuit block constraint function with a value substituted for the selected fan-in cone variable;

generating a second instance of the circuit block constraint function with a complement value substituted for the selected fan-in cone variable; and

ORing the first instance and the second instance.

8. The method of claim 1 wherein the quantifying further comprises:

simplifying the circuit block constraint function using Boolean algebraic derivation to provide the circuit block constraints wherein relations between one or more of the block input variables are provided.

9. The method of claim 1 further comprising:

computing a difference between the at least one circuit block constraint and at least one circuit block user constraint.

10. The method of claim 9 further comprising:

performing equivalence testing on the circuit block using the difference.

11. The method of claim 1 further comprising conjoining an initial state restriction into the circuit block constraint function.

12. The method of claim 1 further comprising:

selecting another circuit block of the circuit, the another circuit block having a second plurality of block inputs;

deriving a fan-in cone function for each block input of the second plurality, each fan-in cone function comprising a corresponding block input variable expressed as a function of at least one fan-in cone variable;

conjoining the fan-in cone functions for each block input of the second plurality into a second circuit block constraint function; and

quantifying the second circuit block constraint function to provide at least one circuit block constraint as a function of block input variables.

13. The method of claim 1 further comprising:

automatically converting the at least one circuit block constraint to an assertion; and

using the assertion during a functional simulation of the circuit block.

14. The method of claim 1 wherein the fan-in cone function for each block input has an equivalence form.

15. The method of claim 1 wherein the circuit block is one of a design specification or a design implementation.

16. The method of claim 1 further comprising:

generating a design specification of the circuit block;

generating a design implementation of the circuit block;

performing equivalence testing of the design implementation and design specification to determine if the design implementation satisfies the design specification.

17. The method of claim 16 wherein the performing equivalence testing is performed accounting for at least some behaviors of the at least one circuit block constraint.

18. The method of claim 17 wherein the performing equivalence testing is performed accounting for all of the behaviors of the at least one circuit block constraint.

19. The method of claim 1 wherein the circuit block constraints of the at least one circuit block constraint are characterized as auto constraints.

20. An apparatus comprising at least one computer aided design tool implemented by the execution of code on at least one computer readable medium, the code comprising:

instructions for deriving a fan-in cone function for each block input of a plurality of inputs of a circuit block, each fan-in cone function comprising a corresponding block input variable expressed as a function of at least one fan-in cone variable;

instructions for conjoining the fan-in cone functions for each block input of the plurality into a circuit block constraint function; and

instructions for quantifying the circuit block constraint function to provide at least one circuit block constraint as a function of block input variables.

21. The apparatus of claim 20 wherein the code further comprises:

instructions for computing a difference between the at least one circuit block constraint and at least one circuit block user constraint.

22. The apparatus of claim 21, wherein the code further comprises:

instructions for performing equivalence testing of the circuit block using the difference.

23. The apparatus of claim 20, wherein the code further comprises:

instructions for performing equivalence testing of the circuit block using the at least one circuit block constraint.

24. The apparatus of claim 20, wherein the code further comprises:

instructions for converting the at least one circuit block constraint to an at least one assertion;

instructions for using the at least one assertion during functional simulation of the circuit block.

25. The apparatus of claim 20 wherein the code further comprises:

instructions for selecting the circuit block from a circuit design.

26. The apparatus of claim 20 wherein the code further comprises:
instructions for conjoining an initial state restriction into the circuit block constraint function.

27. An apparatus for designing a circuit comprising:
means for deriving a fan-in cone function for each block input of a plurality of block inputs of a circuit block, each fan-in cone function comprising a corresponding block input variable expressed as a function of at least one fan-in cone variable;
means for conjoining the fan-in cone functions for each block input into a circuit block constraint function; and
means for quantifying the circuit block constraint function to provide at least one circuit block constraint as a function of block input variables.

28. The apparatus of claim 27 wherein the means for conjoining further comprises:
means for conjoining an initial state restriction into the circuit block constraint function.

29. The apparatus of claim 27 wherein the means for deriving a fan-in cone function further comprises:
means for backtracing each circuit branch of a selected block input of the plurality to a stop node, the stop node being at least one of a latch output, a primary circuit input, a memory output, and an intermediate circuit node if such intermediate circuit node is common to a plurality of fan-in cones corresponding to the circuit block.

30. The apparatus of claim 27 wherein the means for deriving the fan-in cone function further comprises:
means for defining each block input variable for each block input of the plurality to be equivalent to a logical function of fan-in cone variables corresponding to the block input variable, the logical function depending on circuitry in a backtraced circuit branch.

31. The apparatus of claim 27 further comprising:

means for computing a difference between the at least one circuit block constraint and an at least one circuit block user constraint.

32. The apparatus of claim 31 further comprising:

means for performing equivalence testing on the circuit block using the difference.

33. The apparatus of claim 27 further comprising:

means for performing equivalence testing on the circuit block using the at least one circuit block constraint.

34. The apparatus of claim 27 further comprising:

means for automatically converting the at least one circuit block constraint to at least one assertion; and

means for using the at least one assertion during functional simulation of the circuit block.

35. The apparatus of claim 27 further comprising:

means for selecting the circuit block from a circuit.